



Shaheed Rajguru College of Applied Sciences for Women
University of Delhi
Faculty Profile

Name	Dr. Neha Garg	
Designation	Assistant Professor	
Email	neha.garg@rajguru.du.ac.in	
Degree	Institution	Year
Ph.D. (Electronics)	Department of Electronic Science, University of Delhi, South Campus.	2023
M.Sc. Electronics	Department of Electronic Science, University of Delhi, South Campus.	2011
B.Sc. (H) Electronics	University of Delhi, Delhi	2009
NET with JRF (Electronic Science)	University Grant Commission	2012
Areas of Interest / Specialization		
Modelling, Simulation, and Characterization of Advanced Semiconductor Devices for low-power VLSI Design and Sensing Applications.		
Publications Profile		
Publications in International Journals:		
1. Garg, N., Pratap, Y., & Kabra, S. (2025). Investigation of stability parameters of a gate-stack junctionless double-gate transistor (GS-JLDGT)-based 6T and 3T SRAM in the presence of traps. <i>Journal of Computational Electronics</i>, 24, 52. https://doi.org/10.1007/s10825-025-02285-7 2. Babbar, D., Garg, N., & Kabra, S. (2025). Stability analysis and optimization of stack oxide junctionless FinFET based ammonia gas sensor. <i>Microsystem Technologies</i>. https://doi.org/10.1007/s00542-025-05849-6 3. Babbar, D., Garg, N., & Kabra, S. (2025). Designing and reliability assessment of stack oxide double gate junctionless transistor based ammonia gas sensor. <i>Sensing and Imaging</i>, 26, 24. https://doi.org/10.1007/s11220-025-00554-0 4. Babbar, D., Garg, N., & Kabra, S. (2024). Comparative simulation study of InGaN and		

silicon channel stack oxide twin gate field effect transistor based ammonia gas sensor. *Sensing and Imaging*, 25, 20. <https://doi.org/10.1007/s11220-024-00469-2>

5. Babbar, D., Garg, N., & Kabra, S. (2024). Capacitance modeling, simulation and RF characterization of horizontal floating gate field effect transistor (H-FGFET) for gas sensing application. *Engineering Research Express*, 6(2), 025351. <https://doi.org/10.1088/2631-8695/ad51d2>
6. Garg, N., Pratap, Y., & Kabra, S. (2023). Efficient implementation of a DSIG-JLT-based multiplexer and demultiplexer using different logic styles at 20-nm technology. *Journal of Computational Electronics*, 22(6), 1626–1635. <https://doi.org/10.1007/s10825-023-02099-5>
7. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2021). Dielectric separated independent gates junctionless transistor (DSIG-JLT) for highly scaled digital logic implementation. *IEEE Transactions on Nanotechnology*, 20(2), 262–269. <https://doi.org/10.1109/TNANO.2021.3066814>
8. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2020). Reliability assessment of GaAs/Al₂O₃ junctionless FinFET in the presence of interfacial layer defects and radiations. *IEEE Transactions on Device and Materials Reliability*, 20(2), 452–458. <https://doi.org/10.1109/TDMR.2020.2991662>
9. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2019). Impact of different localized trap charge profiles on the short channel double gate junctionless nanowire transistor based inverter and ring oscillator circuit. *AEU – International Journal of Electronics and Communications*, 108, 251–261. <https://doi.org/10.1016/j.aeue.2019.06.014>

Book Chapters:

1. Kabra, S., & Garg, N. (2024). Modelling of kink effects and current collapse in GaN HEMTs. In J. Ajayan & D. Nirmal (Eds.), *Modeling of AlGaIn/GaN high electron mobility transistors*. Springer. <https://doi.org/10.1007/978-981-97-7506-4>
2. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2021). Impact of trap charges and high temperature on reliability of GaAs/Al₂O₃-based junctionless FinFET (pp. 434–440). In N. R. Das & S. Sarkar (Eds.), *Computers and devices for communication: Proceedings of CODEC 2019* (Lecture Notes in Networks and Systems, Vol. 147). Springer. <https://doi.org/10.1007/978-981-15-8366-7>

Publication in International Conferences :

1. Babbar, D., Garg, N., & Kabra, S. (2025). Linearity assessment of gate stack junctionless FinFET based ammonia gas sensor. In *2025 IEEE 6th India Council International Subsections Conference (INDISCON)* (pp. 1–5). IEEE.

<https://doi.org/10.1109/INDISCON66021.2025.11253970>

2. Babbar, D., Garg, N., & Kabra, S. (2024). Sensitivity investigation of gate stack junctionless GaAs FinFET based NH₃ gas sensor. In *2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 737–741). IEEE. <https://doi.org/10.1109/EDKCON62339.2024.10870682>
3. Garg, N., Pratap, Y., & Kabra, S. (2022). Impact of load capacitance and interface trap charges on dynamic behaviour of double-gate junctionless transistor based CMOS inverter. In *2022 IEEE 9th Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON)*. IEEE. <https://doi.org/10.1109/UPCON56432.2022.9986429>
4. Das, N., Dhyani, B., Singh, A., Sehgal, H. D., Garg, N., Kabra, S., & Gautam, N. (2022). Low-cost MOSFET-based pH sensor using Ag/AgCl glass electrodes. In *2022 IEEE 9th Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON)* (pp. 1–5). IEEE. <https://doi.org/10.1109/UPCON56432.2022.9986475>
5. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2021). Stability and reliability performance of double-gate junctionless transistor (DG-JLT) 6T SRAM. In *2021 International Conference on Industrial Electronics Research and Applications (ICIERA)*. IEEE. <https://doi.org/10.1109/ICIERA53202.2021.9726766>
6. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2021). Impact of trap charges and high temperature on reliability of GaAs/Al₂O₃-based junctionless FinFET (pp. 434–440). In N. R. Das & S. Sarkar (Eds.), *Computers and devices for communication: CODEC 2019* (Lecture Notes in Networks and Systems, Vol. 147). Springer. https://doi.org/10.1007/978-981-15-8366-7_64
7. Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2018). Analysis of interface trap charges of double-gate junctionless nanowire transistor (DG-JNT) for digital circuit applications. In *2018 IEEE Electron Devices Kolkata Conference (EDKCON)*. IEEE. <https://doi.org/10.1109/EDKCON.2018.8770427>
8. Sachdeva, T., Aakanksha, Garg, N., Digari, S., Kaira, H., Tiwary, S., Dolly, Neerajpreet Kaur, Goel, B., Naib, P., Jain, C., Jain, S., & Rajan, S. (2017). Designing of an application for group based coordination for information exchange in ad-hoc networks. In *2017 International Conference on Computing and Communication Technologies for Smart Nation (IC3TSN)* (pp. 66–70). IEEE. <https://doi.org/10.1109/IC3TSN.2017.8284452>

Innovation Project Completed:

Completed Innovation project titled “Groups based co-ordination for information exchange in ad-hoc networks” sanctioned by Delhi University in 2015-2016.

Grant mobilized: 4.5 Lakhs

Awards and Distinctions

1. Received the Second Prize for presenting research work at the “Research Conclave”, organized by the Department of Electronic Science, University of Delhi, in collaboration with the IEEE Electron Device Society–Delhi Chapter, under the theme “Electronic Devices & IoT”, in October 2022.
2. Secured First Position in B.Sc.(H) Electronics in College in 2009.